

Claims

1. A field effect transistor, comprising:
 - a substrate;
 - a bottom gate disposed on the substrate;
 - a dielectric disposed on the substrate;
 - a channel disposed above the bottom gate;
 - a source disposed on the dielectric and having a source extension extending from a main body of the source and coupled to the channel;
 - a drain disposed on the dielectric and having a drain extension extending from a main body of the drain and coupled to the channel;
 - a gate insulator disposed on the channel;
 - a top gate disposed on the gate insulator;
 - a first insulating spacer disposed between the top gate and the source and proximate to the source extension; and
 - a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension.
2. The transistor of claim 1, wherein the channel has a cross-sectional U-shape.
3. The transistor of claim 2, wherein the gate insulator has a cross-sectional U-shape.
4. The transistor of claim 1, further comprising:
 - a first local interconnect coupled to the top gate; and
 - a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.

5. The transistor of claim 1, further comprising a local interconnect coupled to the top gate and insulated from the bottom gate.

6. The transistor of claim 1, further comprising a local interconnect coupled to the top gate and coupled to the bottom gate.

7. The transistor of claim 1, wherein the channel is undoped.

8. The transistor of claim 1, wherein the main body of the source and drain is vertically disposed higher than the channel.

9. A method for manufacturing a field effect transistor, comprising:
providing a substrate;
forming a bottom gate on the substrate;
providing a dielectric layer disposed on the substrate;
forming a channel above the bottom gate;
providing a source and drain on the dielectric layer, wherein the source includes a main body and a source extension extending from the main body and coupling to the channel, and the drain includes a main body and a drain extension extending from the main body and coupling to the channel;
forming a gate insulator on the channel;
forming a top gate on the gate insulator;
forming a first insulating spacer between the top gate and the source and proximate to the source extension; and
forming a second insulating spacer between the top gate and the drain and proximate to the drain extension.

10. The method of claim 9, wherein the channel has a cross-sectional U-shape.

11. The method of claim 10, wherein the gate insulator is U-shape.

12. The method of claim 9, further comprising:
forming a first local interconnect coupled to the top gate; and
forming a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.
13. The method of claim 9, further comprising forming a local interconnect coupled to the top gate and insulated from the bottom gate.
14. The method of claim 9, further comprising forming a local interconnect coupled to the top gate and insulated from the bottom gate.
15. The method of claim 9, wherein the main body of the source and drain is vertically disposed higher than the channel.
16. The method of claim 9, wherein forming the source and drain includes doping a silicon material to form an N⁺ region defining the source and drain.
17. A field effect transistor, comprising:
a substrate;
a bottom gate disposed on the substrate;
a dielectric disposed on the substrate;
a channel disposed above the bottom gate;
a source disposed on the dielectric and having a source extension extending from a main body of the source and coupled to the channel;
a drain disposed on the dielectric and having a drain extension extending from a main body of the drain and coupled to the channel;
a gate dielectric insulator disposed on the channel;
a top gate disposed on the gate dielectric insulator;
a first insulating spacer disposed between the top gate and the source and proximate to the source extension;

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension;

a local interconnect disposed on the top gate and between the first and second spacers;

a first pad disposed on the source;

a second pad disposed on the drain;

a first contact extending through the first pad and coupled to the source; and

a second contact extending through the second pad and coupled to the drain.

18. The transistor of claim 17, wherein the channel has a cross-sectional U-shape.

19. The transistor of claim 18, wherein the gate dielectric insulator has a cross-sectional U-shape.

20. The transistor of claim 17, further comprising a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.

21. The transistor of claim 17 wherein the local interconnect is insulated from the bottom gate.

22. The transistor of claim 17, wherein the local interconnect is coupled to the bottom gate.

23. The transistor of claim 17, wherein the channel is undoped.

24. The transistor of claim 17, wherein the main body of the source and drain is vertically disposed higher than the channel.

25. The transistor of claim 17, further comprising a plurality of exterior spacers disposed on the substrate and proximate to the dielectric layer, source, drain, and pads.

26. The transistor of claim 25, further comprising an insulator layer disposed on the substrate and coupled to the exterior spacers.

27. The transistor of claim 17 further comprising an ILD layer disposed on the first and second pads and wherein the first and second contacts extend through the ILD layer.

28. A field effect transistor, comprising:

a substrate;

bottom gate control means disposed on the substrate for effecting gate control;

a dielectric disposed on the substrate;

channel means disposed above the bottom gate for providing an electron flow;

a source disposed on the dielectric and having a source extension extending from a main body of the source and coupled to the channel means;

a drain disposed on the dielectric and having a drain extension extending from a main body of the drain and coupled to the channel means;

a gate dielectric insulator disposed on the channel means;

a top gate control means disposed on the gate dielectric insulator for effecting gate control;

a first spacer disposed between the top gate control means and the source and proximate to the source extension; and

a second spacer disposed between the top gate control means and the drain and proximate to the drain extension.

29. The transistor of claim 28, wherein the channel means has a cross-sectional U-shape.

30. The transistor of claim 29, wherein the gate dielectric insulator has a cross-sectional U-shape.

31. A double-gated field effect transistor having independent gate control, comprising:

- a substrate;
- a bottom gate disposed on the substrate;
- a dielectric disposed on the substrate;
- a channel disposed above the bottom gate;
- a source disposed on the dielectric and having a source extension extending from a main body of the source and coupled to the channel;
- a drain disposed on the dielectric and having a drain extension extending from a main body of the drain and coupled to the channel;
- a gate dielectric insulator disposed on the channel;
- a top gate disposed on the gate dielectric insulator;
- a first insulating spacer disposed between the top gate and the source and proximate to the source extension;
- a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension;
- a first local interconnect coupled to the top gate and disposed between the first and second spacers; and
- a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.

32. The transistor of claim 31, wherein the channel has a cross-sectional U-shape.

33. The transistor of claim 32, wherein the gate dielectric insulator has a cross-sectional U-shape.

34. A radiation-resistant field effect transistor, comprising:

a substrate;

a bottom gate disposed on the substrate;

a nitride dielectric disposed on the substrate;

a channel disposed above the bottom gate;

a source disposed on the dielectric to prevent contact with the substrate, the source coupled to the channel;

a drain disposed on the dielectric to prevent contact with the substrate, the drain coupled to the channel;

a gate insulator disposed on the channel;

a top gate disposed on the gate insulator; and

a plurality of nitride exterior spacers disposed on the substrate and surrounding the bottom gate, dielectric, source, drain, gate insulator and top gate.

35. The field effect transistor of claim 34, further comprising:

a first nitride pad disposed on the source; and

a second nitride pad disposed on the drain.

36. The field effect transistor of claim 35, further comprising:

a first contact extending through the first nitride pad and coupled to the source; and

a second contact extending through the second nitride pad and coupled to the drain.

37. The field effect transistor of claim 34, wherein,

the source includes a source extension extending from a main body of the source and coupled to the channel;

the drain includes a drain extension extending from a main body of the drain and coupled to the channel;

a first insulating spacer disposed between the top gate and the source and proximate to the source extension; and

a second insulating spacer disposed between the top gate and the drain and proximate to the drain extension.

38. The field effect transistor of claim 34, wherein the channel has a cross-sectional U-shape.

39. The field effect transistor of claim 34, wherein the gate dielectric insulator has a cross-sectional U-shape.

40. The field effect transistor of claim 34 further comprising a local interconnect coupled to the top gate.

41. The field effect transistor of claim 40, further comprising a second local interconnect insulated from the first local interconnect and coupled to the bottom gate to provide independent bias to the bottom gate.

42. The field effect transistor of claim 40 wherein the local interconnect is insulated from the bottom gate.

43. The field effect transistor of claim 40, wherein the local interconnect is coupled to the bottom gate.

44. The field effect transistor of claim 34, wherein the channel is undoped.